

AMENDMENTS TO THE CLAIMS

Claim 1 (Currently Amended): A semiconductor memory device, comprising:

a cell area having N+1 number of unit cell blocks, each including M number of word lines wherein the N number of unit cell blocks are each corresponded to a logical cell block address and one unit cell block is added for accessing data with high speed;

a predetermined cell block table for storing a candidate information representing at least more than one candidate word line among the ~~M~~ M * (N+1) number of the word lines ~~to be stored data;~~ and

a tag block for receiving a row address, sensing a the logical cell block address in the row address and outputting a physical cell block address based on the logical cell block address and the candidate information,

wherein the tag block includes:

N+1 number of unit tag tables corresponding to the N+1 number of unit cell blocks, each having M number of registers, ~~and storing a store information that the M number of registers corresponds~~ corresponding to M number of word lines of corresponding unit cell blocks, each register storing one of ~~N number of~~ logical cell block address ~~each the physical unit cell block address in response to the logical cell block among unit cell block addresses having a word line in response to the candidate information;~~ and

an initialization unit for initializing the N+1 number of unit tag tables.

Claim 2 (Currently Amended): The semiconductor memory device as recited in claim 1, further comprising:

a control means for controlling the tag block and the predetermined cell block table for activating one word line of a unit cell block selected by the physical cell block address.

Claim 3 (Currently Amended): The semiconductor memory device as recited in claim 1, wherein the initialization unit includes:

a plurality of logical OR gates respectively corresponding to the N+1 number of unit cell blocks for respectively receiving an initialization enable ~~selection~~ signal to ~~initialize~~ enable the

N+1 number of unit tag tables and a tag table selection signal to select one of the N+1 number of unit tag tables and respectively outputting ~~each of~~ a corresponding initialization activating signals to ~~each of~~ the N+1 number of corresponding unit tag tables;

a plurality of first multiplexers controlled by the initialization selection signal and respectively corresponding to the N+1 number of unit cell blocks for selectively outputting one ~~between of~~ the input logical cell block address and ~~each of~~ an initialization signals to initialize each corresponding unit tag tables of the N+1 number of unit tag tables ~~to each of the N+1 number of unit tag tables~~; and

a plurality of second multiplexers controlled by the initialization selection signal and respectively corresponding to the N+1 number of unit cell blocks for selectively outputting one ~~between of~~ a local address to select one of M number of word lines of corresponding unit cell blocks ~~included in each of the N+1 number of unit cell blocks~~ and an initialization address to select all registers ~~included in one of the unit tag table~~ the corresponding unit tag table.

Claim 4 (Currently Amended): A method for controlling a tag block for assigning a physical unit cell address based on a logical unit cell block, comprising ~~the steps of~~:

a) initializing the tag block in a semiconductor memory device; and
b) performing a ~~normal~~ data access operation of the semiconductor memory device by using the tag block,

wherein a) ~~the~~ initializing the tag block in a semiconductor memory device including:

a-1) nullifying ~~the~~ a N+1 number of unit tag tables of the tag block;
a-2) selecting all the N+1 number of unit tag tables; and
a-3) storing each different logical unit cell block information in the N number of unit tag tables among the N+1 number of unit tag tables.

Claim 5 (Canceled)

Claim 6 (New): A method for a refresh operation of a semiconductor memory device including a cell area having $N+1$ number of unit cell blocks, each including M number of word lines which respectively are coupled to a plurality of unit cells; a tag block having $N+1$ number of unit tag blocks, each having M number of registers for sensing an update of data, comprising:

 nullifying the $N+1$ number of unit tag tables;

 selecting all the $N+1$ number of unit tag tables; and

 storing each different logical unit cell block information in the N number of unit tag tables among the $N+1$ number of unit tag tables,

 wherein the N number of unit cell blocks are corresponded to an address and one unit cell block is added for accessing data with high speed.